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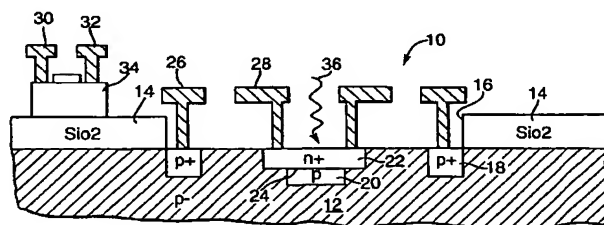
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- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Declaration under Rule 4.17:**
— of inventorship (Rule 4.17(iv)) for US only
- Published:**
— with international search report

[Continued on next page]

(54) Title: PHOTODETECTOR CIRCUITS



(57) Abstract: A photodetector circuit incorporates an APD detector structure (10) comprising a p- silicon handle wafer (12) on which a SiO₂ insulation layer (14) is deposited in known manner. During manufacture a circular opening (16) is formed through the insulation layer (14) by conventional photolithography and etching, and an annular p⁺ substrate contact ring (18) is implanted in the handle wafer (12) after opening of the window (16). The APD itself is formed by implantation of a p region (20) and an n⁺ region (22). After the various implantation steps a metallisation layer is applied, and annular metal contacts are formed by the application of suitable photolithography and etching steps, these contacts comprising an annular contact (26) constituting the negative terminal and connected to the p⁺ substrate contact ring (18), an annular metal contact (28) constituting the positive terminal and connected to the n⁺ region (22) of the APD, and source and drain contacts (30 and 32) connected to the source and drain of one or more CMOS MOSFET devices of the associated CMOS readout circuitry fabricated within a Si layer (34) formed on top of the insulation layer (14). Such an arrangement overcomes the problem of combining APDs with CMOS circuits in that APDs operate at relatively high reverse bias (15-30V) and CMOS circuits operate at low voltage (5V).



— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(88) Date of publication of the international search report:
23 September 2004

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference IP/P7153/WOD	FOR FURTHER ACTION see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/GB 03/02851	International filing date (day/month/year) 03/07/2003	(Earliest) Priority Date (day/month/year) 11/07/2002
Applicant QINETIQ LIMITED		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 7 sheets.

☒ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. ☐ **Certain claims were found unsearchable** (See Box I).

3. ☒ **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☐ the text is approved as submitted by the applicant.

☒ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No.

☒ as suggested by the applicant.

☐ because the applicant failed to suggest a figure.

☐ because this figure better characterizes the invention.

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☐ None of the figures.

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Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

A photodetector circuit incorporates an APD detector structure (10) comprising a p-silicon handle wafer (12) on which a SiO₂ insulation layer (14) is deposited in known manner. During manufacture a circular opening (16) is formed through the insulation layer (14) by conventional photolithography and etching, and an annular p+ substrate contact ring (18) is implanted in the handle wafer (12) after opening of the window (16). The APD itself is formed by implantation of a p region (20) and an n+ region (22). After the various implantation steps a metallisation layer is applied, and annular metal contacts are formed by the application of suitable photolithography and etching steps, these contacts comprising an annular contact (26) constituting the negative terminal and connected to the p+ substrate contact ring (18), an annular metal contact (28) constituting the positive terminal and connected to the n+ region (22) of the APD, and source and drain contacts (30 and 32) connected to the source and drain of one or more CMOS MOSFET devices of the associated CMOS readout circuitry fabricated within a Si layer (34) formed on top of the insulation layer (14). Such an arrangement overcomes the problem of combining APDs with CMOS circuits in that APDs operate at relatively high reverse bias (15-30V) and CMOS circuits operate at low voltage (5V).

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/GB 03/02851

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L27/14 H01L27/146 H01L31/107 H01L31/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/024058 A1 (BIRCH STEVEN W ET AL) 28 February 2002 (2002-02-28) paragraphs '0101! - '0103!, '0110!, '0111!; claims 1,2; figures 16,19,20	1-4,6-9, 12-15, 18,19, 24,25
Y		20
X	US 5 786 615 A (SAITO YUTAKA) 28 July 1998 (1998-07-28) column 3, line 19 - column 4, line 51; figure 11 ----- -/--	1-3,24, 25

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

G document member of the same patent family

Date of the actual completion of the international search

26 July 2004

Date of mailing of the international search report

02/08/2004

Name and mailing address of the ISA

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Voignier, V

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 03/02851

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	XU C ET AL: "A LOW VOLTAGE HYBRID BULK/SOI CMOS ACTIVE PIXEL IMAGE SENSOR" May 2001 (2001-05), IEEE ELECTRON DEVICE LETTERS, IEEE INC. NEW YORK, US, PAGE(S) 248-250 , XP001086943 ISSN: 0741-3106 the whole document	1-3, 24, 25
Y	FR 2 742 878 A (COMMISSARIAT ENERGIE ATOMIQUE) 27 June 1997 (1997-06-27) abstract; figure 2	20
A	MOLONEY A M ET AL: "Small signal equivalent circuit for Geiger-mode avalanche photodiodes" 14 March 2002 (2002-03-14), ELECTRONICS LETTERS, IEE STEVENAGE, GB, PAGE(S) 285-286 , XP006017928 ISSN: 0013-5194 the whole document	1-3
A	NORIYOSHI YAMAUCHI ET AL: "AN INTEGRATED PHOTODETECTOR-AMPLIFIER USING A-SI P-I-N PHOTODIODES AND POLY-SI THIN-FILM TRANSISTORS" 1 March 1993 (1993-03-01), IEEE PHOTONICS TECHNOLOGY LETTERS, IEEE INC. NEW YORK, US, PAGE(S) 319-321 , XP000362935 ISSN: 1041-1135 figure 2	9, 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB 03/02851

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this International application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-11,18,19,24,25

A photodetector circuit including a Avalanche Photodiode comprising two regions of opposite conductivity formed in the substrate, and a readout circuit formed on an insulating layer deposited on the substrate.

A method to fabricate the photodetector circuit.

2. claims: 12-14

A photodetector circuit including a Photodiode comprising two regions of opposite conductivity formed in the substrate and one epitaxial layer formed on the substrate, and a readout circuit supported by and isolated from the substrate.

3. claims: 15-17,20-23

A photodetector circuit including a Photodiode comprising a junction formed in the substrate, and a readout circuit formed on an insulating layer deposited on the substrate, the photodiode being formed in a thinned portion of the substrate so that it can detect light incident on the back surface of the substrate.

A method of making the photodetector circuit.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/GB 03/02851

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 2002024058	A1	28-02-2002	GB	2367945 A	17-04-2002
			TW	543197 B	21-07-2003
US 5786615	A	28-07-1998	JP	3363561 B2	08-01-2003
			JP	6314699 A	08-11-1994
			EP	0614229 A2	07-09-1994
FR 2742878	A	27-06-1997	FR	2742878 A1	27-06-1997
			DE	69626547 D1	10-04-2003
			DE	69626547 T2	19-02-2004
			EP	0870335 A1	14-10-1998
			WO	9723003 A1	26-06-1997
			JP	2000510649 T	15-08-2000